

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
6 June 2002 (06.06.2002)

PCT

(10) International Publication Number
WO 02/45156 A2

(51) International Patent Classification⁷: **H01L 21/8238**

(21) International Application Number: **PCT/US01/44162**

(22) International Filing Date:
6 November 2001 (06.11.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/727,296 29 November 2000 (29.11.2000) US

(71) Applicant (for all designated States except US): **INTEL CORPORATION [US/US];** 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **ARMSTRONG, Mark [US/US];** 2861 NW Adagio Way, Hillsboro, OR 97124 (US). **SCHROM, Gerhard [US/US];** 7008 NE Ronler Way, #3225, Hillsboro, CA 97124 (US). **KUHN,**

Kelin, J. [US/US]; 20280 SW Clarion Street, Aloha, OR 97006 (US). **PACKAN, Paul, A. [US/US];** 15025 SW Gibractor Court, Beaverton, OR 97007 (US). **TYAGI, Sunit, D. [IN/US];** 17555 NW Waltuck Court, Portland, OR 97229 (US). **THOMPSON, Scott, E. [US/US];** 18635 NW Rock Creek Way, Portland, OR 97229 (US).

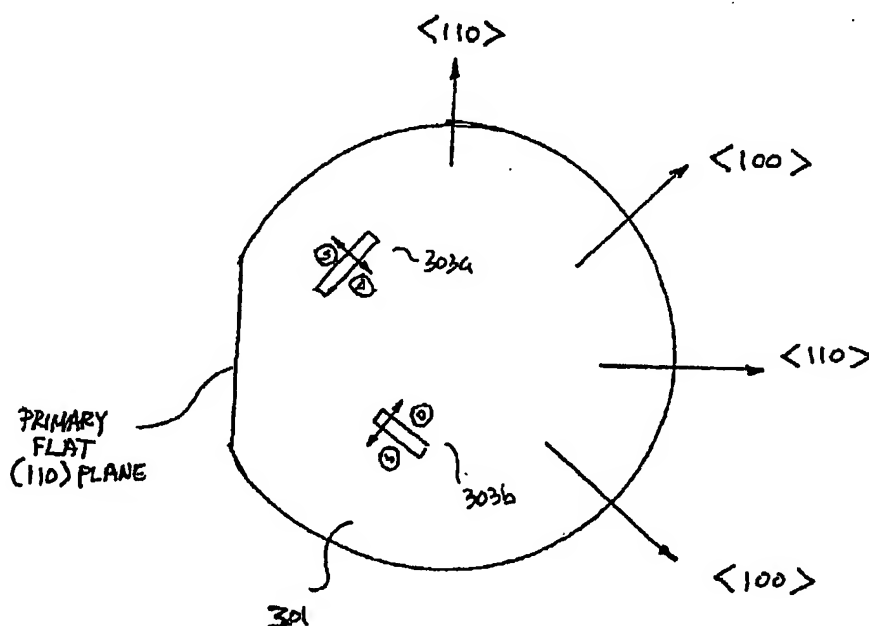
(74) Agents: **MALLIE, Michael, J. et al.;** Blakely, Sokoloff, Taylor & Zafman, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, CA 90025 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE,

[Continued on next page]

(54) Title: **CMOS FABRICATION PROCESS UTILIZING SPECIAL TRANSISTOR ORIENTATION**



(57) Abstract: Complementary metal oxide semiconductor transistors are formed on a silicon substrate. The substrate has a {100} crystallographic orientation. The transistors are formed on the substrate so that current flows in the channels of the transistors are parallel to the <100> direction. Additionally, longitudinal tensile stress is applied to the channels.

WO 02/45156 A2

WO 02/45156 A2



IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

- *without international search report and to be republished upon receipt of that report*

BEST AVAILABLE COPY

CMOS FABRICATION PROCESS UTILIZING SPECIAL TRANSISTOR ORIENTATION

6

Technical Field of the Invention

The present invention relates to semiconductor transistors, and more particularly, to a transistor structure oriented having a current flow parallel to a specific crystal direction.

Background of the Invention

Complementary metal oxide semiconductor (CMOS) integrated circuits include both N-type devices (NMOS) and P-type devices (PMOS), the former utilizing electrons as the carriers and the latter utilizing holes as the carriers. CMOS technology is employed in the large majority of integrated circuits manufactured today.

An important factor in the performance of CMOS integrated circuits is the presence of good mobility for both holes and electrons. The mobility of both carriers should be as high as possible to enhance both PMOS and NMOS performance. The overall CMOS circuit performance depends similarly on both NMOS and PMOS performance, and thus in turn, on both electron and hole mobility.

It is known that the application of stress on a semiconductor material, such as silicon, changes the mobility of electrons and holes, which in turn modifies the performance of NMOS and PMOS devices formed thereon. An increase in mobility results in increased performance. However, it has also been found that the electron and hole mobilities do not always react the same way to stress, thereby complicating the process. In addition, the dependence of mobility on stress depends on the surface orientation of the crystalline semiconductor material and the directions of stress and current flow. For example, for current flow along the $\langle 110 \rangle$ directions on $\{100\}$ planes,

longitudinal tensile stress tends to increase the mobility of electrons and decrease the mobility of holes. In contrast, for current flow along the $\langle 100 \rangle$ directions on $\{100\}$ planes, longitudinal tensile stress tends to increase the mobility of both electrons and holes.

5 Currently, semiconductor devices are oriented such that the current flows along the $\langle 110 \rangle$ direction on $\{100\}$ silicon. This can be seen in Figure 2, which shows a top view of a semiconductor wafer 201. The semiconductor wafer 201 is commonly referred to as " $\{100\}$ silicon," which is the predominant type of semiconductor wafer being used today. In the prior art, NMOS and PMOS transistors 203 are oriented in such a manner so that the
10 current flow between source and drain is aligned with the $\langle 110 \rangle$ direction, relative to the semiconductor wafer 201. Thus, the transistors 203 are oriented as shown in Figure 2.

 In this orientation, the mobilities of electrons and holes change inversely in reaction to longitudinal stress. In other words, when stress is applied to the underlying silicon along the direction of current flow, either the electron mobility is increased and the
15 hole mobility is decreased or the hole mobility is increased and the electron mobility is decreased. Thus, in such an arrangement, the overall CMOS circuit performance is not enhanced.

 For this reason, selective stressing of the silicon material must be employed to increase the carrier mobility of one type of device without degrading the mobility of the
20 other type of device. Thus, stress may be applied to the wafer 201 in the location of transistor 203a, but not transistor 203b, or vice versa. This requires costly processing steps that may include masking, deposition, or etching.

Brief Description of the Drawings

Figure 1 is a schematic diagram showing the three types of crystalline orientation for silicon.

Figure 2 is a schematic diagram showing a prior art orientation of CMOS devices
5 on a semiconductor wafer.

Figure 3 is a schematic diagram showing an orientation of CMOS devices on a semiconductor wafer in accordance with the present invention.

Figure 4A is a chart showing the piezoresistive coefficients for a P-type {100} silicon substrate as a function of current flow direction.

10 Figure 4B is a chart showing the piezoresistive coefficients for an N-type {100} silicon substrate as a function of current flow direction.

Figure 5 shows a transistor that is undergoing longitudinal tensile stress.

Figure 6 shows a transistor that is undergoing transverse tensile stress.

Detailed Description

Silicon (Si) is presently the most important semiconductor for the electronics industry. Most silicon that is used to form silicon wafers is formed from single crystal silicon. The silicon wafers serve as the substrate on which CMOS devices are formed. The silicon wafers are also referred to as a semiconductor substrate or a semiconductor wafer.

In crystalline silicon, the atoms which make up the solid are arranged in a periodic fashion. If the periodic arrangement exists throughout the entire solid, the substance is defined as being formed of a single crystal. If the solid is composed of a myriad of single crystal regions the solid is referred to as polycrystalline material.

Silicon, as used in integrated circuits, can be in one of three forms: (1) single crystal silicon, (2) polycrystalline silicon (polysilicon), and (3) amorphous silicon. As noted above, silicon wafers are fabricated to have single crystal form.

The periodic arrangement of atoms in a crystal is called the lattice. The crystal lattice also contains a volume which is representative of the entire lattice and is referred to as a unit cell that is regularly repeated throughout the crystal.

Silicon has a diamond cubic lattice structure, which can be represented as two interpenetrating face centered cubic lattices. Thus, the simplicity of analyzing and visualizing cubic lattices can be extended to characterization of silicon crystals. In the description herein, references to various planes in silicon crystals will be made, especially to the $\{100\}$, $\{110\}$, and $\{111\}$ planes.

These planes describe the orientation of the plane of silicon atoms relative to the principle crystalline axes. The numbers $\{xyz\}$ are referred to as Miller indices and are determined from the reciprocals of the points at which the crystal plane of silicon intersects the principle crystalline axes. Thus, Figure 1 shows three orientations of the crystal plane of silicon. In Figure 1(A), the crystal plane of silicon intersects the x-axis at 1 and never intersects the y or z-axis. Therefore, the orientation of this type of crystalline silicon is $\{100\}$. Similarly, Figure 1(B) shows $\{110\}$ crystalline silicon and Figure 1(C) shows $\{111\}$ silicon. The $\{111\}$ and $\{100\}$ orientations are the two primary wafer orientations in commercial use.

Note that for any given plane in a cubic crystal there are five other equivalent planes. Thus, the six sides of the cube comprising the basic unit cell of the crystal are all considered $\{100\}$ planes. The notation $\{xyz\}$ refers to all six of the equivalent planes.

Reference will also be made herein to the crystal directions, especially the $\langle 100 \rangle$, $\langle 110 \rangle$ and $\langle 111 \rangle$ directions. These are defined as the normal direction to the respective plane. Thus, the $\langle 100 \rangle$ direction is the direction normal to the $\{100\}$ plane. The notation $\langle xyz \rangle$ refers to all six equivalent directions.

As noted above, in the prior art, most MOS transistors are fabricated on $\{100\}$ silicon with the gates oriented such that current flows parallel to the $\langle 110 \rangle$ directions. This is shown in Figure 2.

In accordance with the present invention, the MOS transistors are oriented so that current flow is substantially along the $\langle 100 \rangle$ direction as shown in Figure 3. Figure 3 shows a top view of a semiconductor wafer 301 formed from $\{100\}$ silicon. Transistor devices, formed on the semiconductor wafer 301, are represented by transistors 303a and 303b. The orientation of the transistors 303a and 303b are such that current that flows between the source and drain of the transistors is substantially along the $\langle 100 \rangle$ direction of the semiconductor wafer 301. Clearly, the transistors 303a and 303b are not drawn to scale and are meant to be exemplary.

Thus, in accordance with one embodiment of the present invention, devices formed on the silicon wafer have a specific device orientation and a fabrication process is used that induces longitudinal tensile stress in the channel region of the devices. The longitudinal tensile stress on the channel will increase the mobility of electrons without degrading the mobility of holes.

In the prior art, devices were oriented such that the current flows substantially along the $\langle 110 \rangle$ directions on $\{100\}$ silicon. In this orientation, the mobilities of electrons and holes change in opposite directions in reaction to longitudinal tensile stress. Thus, the overall CMOS circuit performance is not enhanced. For this reason, selective stressing is

employed to increase the carrying mobility of one type of device without degrading the other. This requires costly processing steps.

By orienting the devices to have their current flow in the $\langle 100 \rangle$ direction, this reduces or reverses the relative degradation of one carrier mobility commensurate with a given amount of increase in the mobility of the other type of carrier due to stress. This eliminates the need for selective stressing to realize an acceptable overall performance gain. The orientation of the present invention enables stress to be used as a tool to increase CMOS circuit performance.

The piezoresistive coefficients for silicon are anisotropic relative to the direction of current flow. Figure 4a shows the piezoresistive coefficient for a p-type region of a semiconductor substrate and Figure 4b shows the piezoresistive coefficient for an n-type region of a semiconductor substrate as a function of direction of current flow on the $\{100\}$ surfaces. NMOS transistors are known to behave similarly to n-type regions and have similar piezoresistive coefficients, as do PMOS transistors and p-type regions. Thus, Figures 4a and 4b are applicable to NMOS and PMOS transistors.

The piezoresistive coefficients relate the change in resistance along various directions when stress is applied. Positive values indicate an increase in resistance for tensile stress. The change in resistance is inversely proportional to the change in mobility, which is directly proportional to the speed of the transistor. Thus, a higher resistance results in a slower transistor.

A longitudinal tensile stress is defined as a "stretching" of the channel in the same direction in which current flows. For example, as seen in Figure 5, a transistor 601 is seen that has a gate 603, a source 605, and a drain 607. When an appropriate voltage is applied to the gate 603, current flows between the source 605 and the drain 607 along the direction

arrow 609. A longitudinal tensile stress would be stress that tends to move the source 605 and drain 607 apart along direction 609. Additionally, a longitudinal compressive stress would be stress that tends to move the source 605 and drain 607 closer together along direction 609.

A transverse tensile stress is defined as a "stretching" of the channel in a direction orthogonal to which the current flows. For example, as seen in Figure 6, a transistor 701 is seen that has a gate 703, a source 705, and a drain 707. When an appropriate voltage is applied to the gate 703, current flows between the source 705 and the drain 707 along the direction arrow 709. A transverse tensile stress would be stress that is in a direction 711 that is orthogonal to the direction of current flow 709.

As seen in Figure 4b, when a longitudinal tensile stress (as indicated by solid line 401) is applied to an n-type region of a semiconductor wafer, the piezoresistive coefficient is at a minimum (approx -100 units) in the $\langle 100 \rangle$ direction. As seen in Figure 4a, when the same longitudinal tensile stress (as indicated by solid line 403) is applied to a p-type region of the semiconductor wafer, the piezoresistive coefficient is only slightly above the neutral condition (0 units).

Thus, in accordance with one embodiment of the present invention, transistors should be oriented to have current flowing in the $\langle 100 \rangle$ direction and applying longitudinal tensile stress in the $\langle 100 \rangle$ direction. This will result in an increase in the speed of NMOS transistors without affecting the PMOS transistors. This is preferable to the $\langle 110 \rangle$ orientation of the prior art, where the PMOS transistor is degraded with the addition of such stress, necessitating a cumbersome selective stress processing to enable an overall gain.

In accordance with an alternative embodiment, it is possible to orient the transistor devices to have current flow in the $\langle 110 \rangle$ direction while applying a transverse stress (as indicated by the dashed lines 405 and 407). For PMOS transistors, this gives about a -70 value and for NMOS transistors, this gives about a -25 value. However, in practice, this is difficult to accomplish because transistors are typically many times wider than they are long. Thus, a force applied on the side of the channel, which would cause transverse stress, is greatly diminished in the middle of the channel.

The particular details of introducing a longitudinal tensile stress on a substrate are well known in the art and will not be discussed in detail herein. For example, in one embodiment, application of high-tensile nitride dielectric is used. The high-tensile nitride dielectric is also referred to herein as a "stressor" structure that will implement the tensile stress. Alternatively, in another embodiment, the stressor structure may be a tensile shallow trench isolation (STI) fill. Although two examples of stressors are given as an example, the term "stressor" as used herein shall mean any structure that causes tensile stress. Additionally, the formation of transistors oriented to have their current flow in the $\langle 100 \rangle$ direction is relatively straightforward. This can be done, for example, by rotating either the underlying semiconductor wafer or the production masks 45 degrees relative to the prior art orientation (for a $\{100\}$ silicon wafer).

While specific embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise configuration and components disclosed herein. Various modifications, changes, and variations, which will be apparent to those skilled in the art, may be made in the
5 arrangement, operation, and details of the methods and systems of the present invention disclosed herein without departing from the spirit and scope of the invention.

These modifications can be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a NMOS device formed on a semiconductor substrate;

a PMOS device formed on said semiconductor substrate, wherein said NMOS device and said PMOS device are oriented so that the current flows in a <100> direction of

5 said semiconductor substrate.

2. The integrated circuit of Claim 1 wherein said semiconductor substrate is formed from {100} silicon.

- 10 3. The integrated circuit of Claim 1 wherein at least a portion of said semiconductor substrate is under a tensile stress.

4. The integrated circuit of Claim 3 wherein said tensile stress is a longitudinal tensile stress.

15

5. The integrated circuit of Claim 4 wherein said longitudinal tensile stress is induced by a high-tensile nitride dielectric or a tensile shallow trench isolation fill.

6. The integrated circuit of Claim 1 wherein said devices are transistors.

20

7. An apparatus comprising:

a semiconductor substrate formed from {100} silicon;

a PMOS transistor formed on said semiconductor substrate, said PMOS transistor having a PMOS channel for carrying current and oriented so that current flows in a <100> direction;

a NMOS formed on said semiconductor substrate, said NMOS transistor having a
5 NMOS channel for carrying current and oriented so that current flows in a <100> direction; and

a stressor that causes a longitudinal tensile stress on said NMOS channel or said PMOS channel.

10 8. The integrated circuit of Claim 7 wherein said stressor is a high-tensile nitride dielectric or a tensile shallow trench isolation fill.

9. The integrated circuit of Claim 7 wherein said devices are transistors.

15 10. A method comprising:

forming a NMOS device on a semiconductor substrate, wherein said NMOS device is oriented so that the current flows in a <100> direction of said semiconductor substrate; and

forming a PMOS device on said semiconductor substrate, wherein said PMOS
20 device is oriented so that the current flows in said <100> direction of said semiconductor substrate.

11. The method of Claim 10 wherein said semiconductor substrate is formed from {100} silicon.

12. The method of Claim 10 further including introducing a tensile stress on at least a portion of said semiconductor substrate.
- 5 13. The method of Claim 12 wherein said tensile stress is a longitudinal tensile stress.
14. The method of Claim 13 wherein said introducing of said longitudinal tensile stress is by use of a stressor.
- 10 15. The method of Claim 14 wherein said stressor is a high-tensile nitride dielectric or a tensile shallow trench isolation fill.

1/6

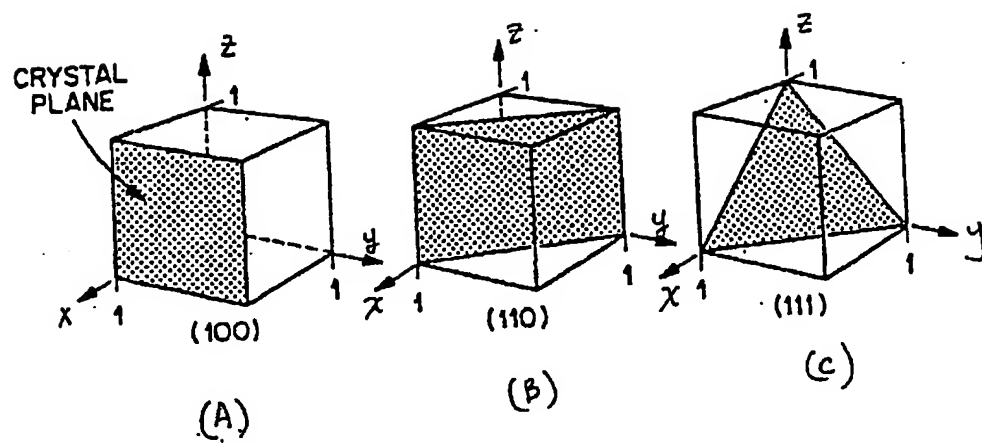


Figure 1
(PRIOR ART)

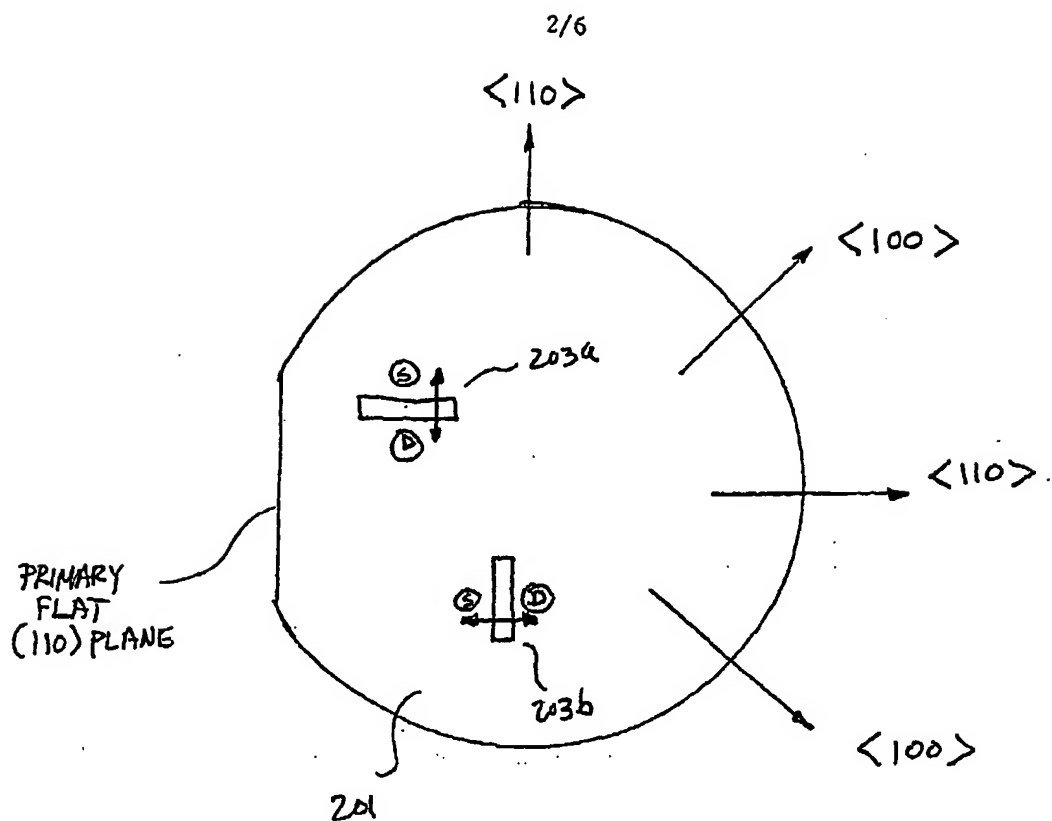


FIGURE 2
(PRIOR ART)

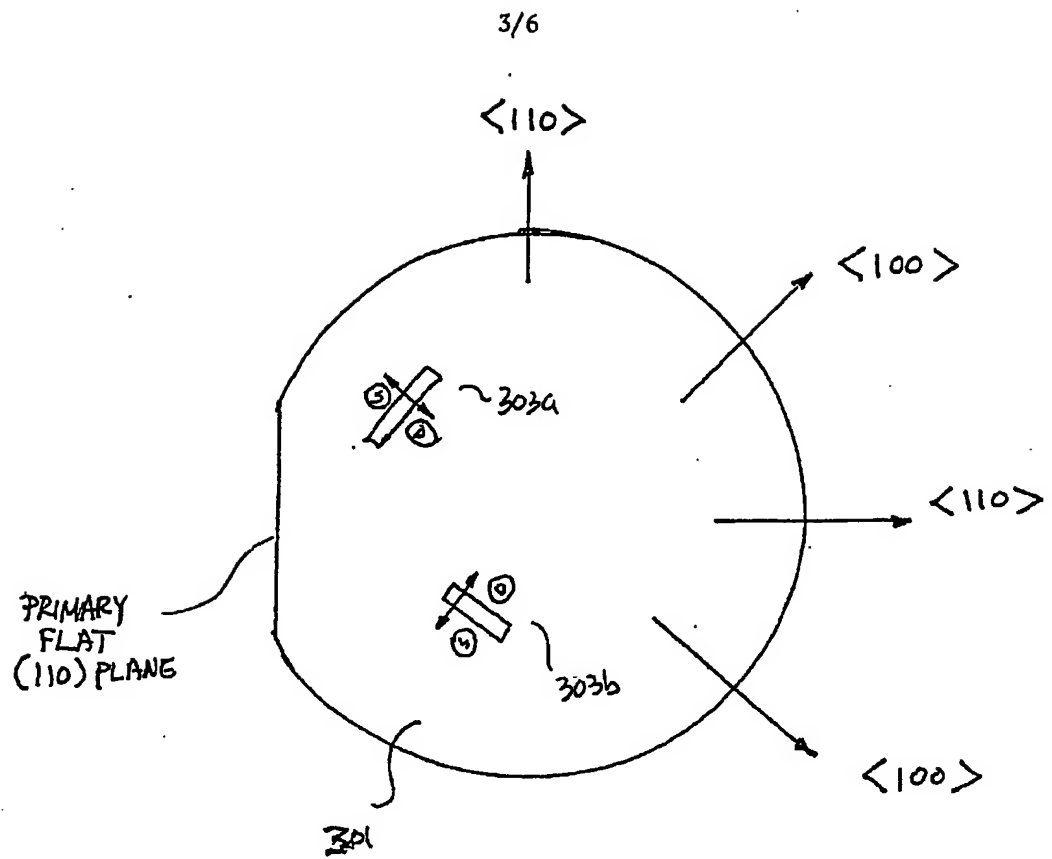


FIGURE 3

4/6

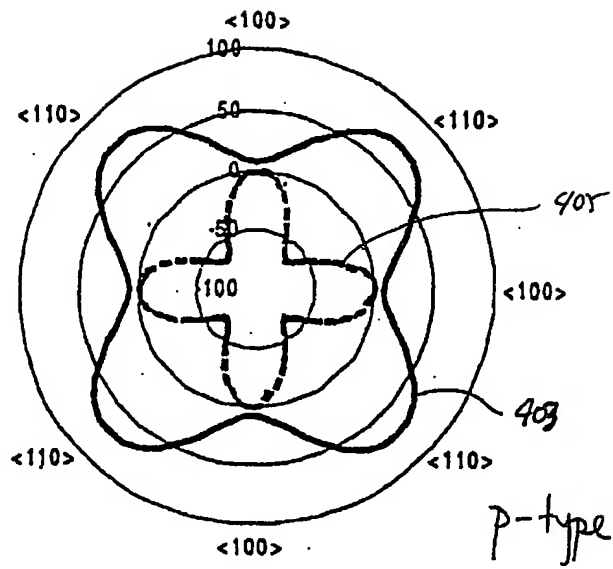


Figure 4A

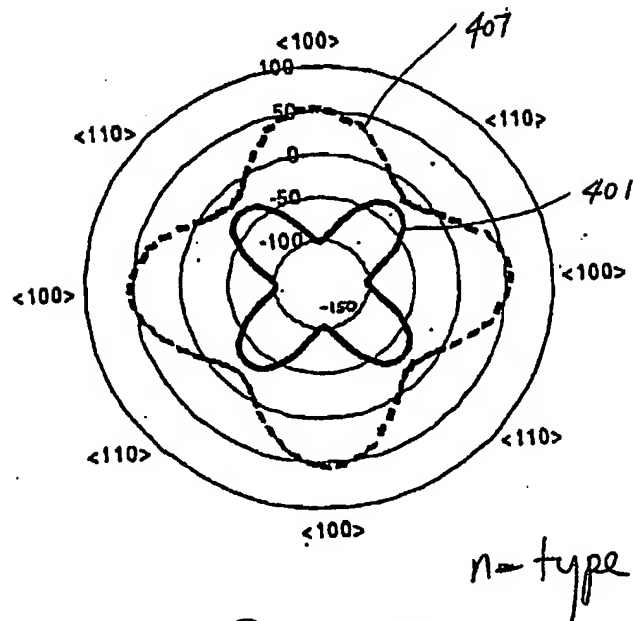


Figure 4B

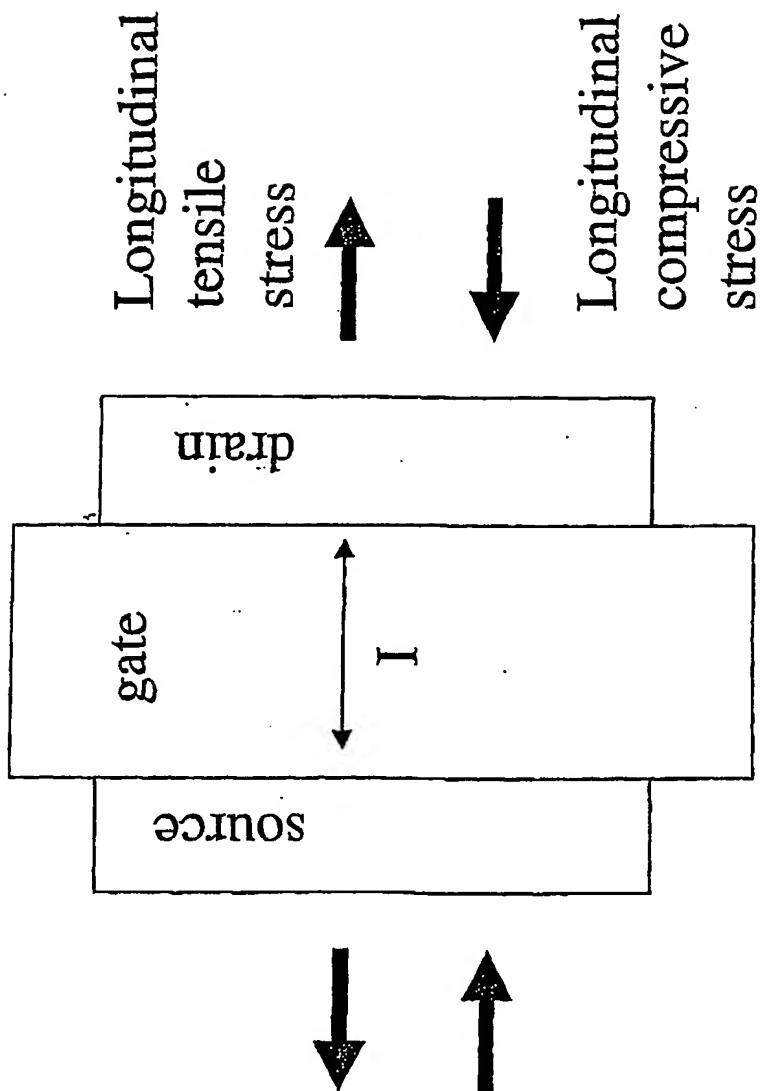
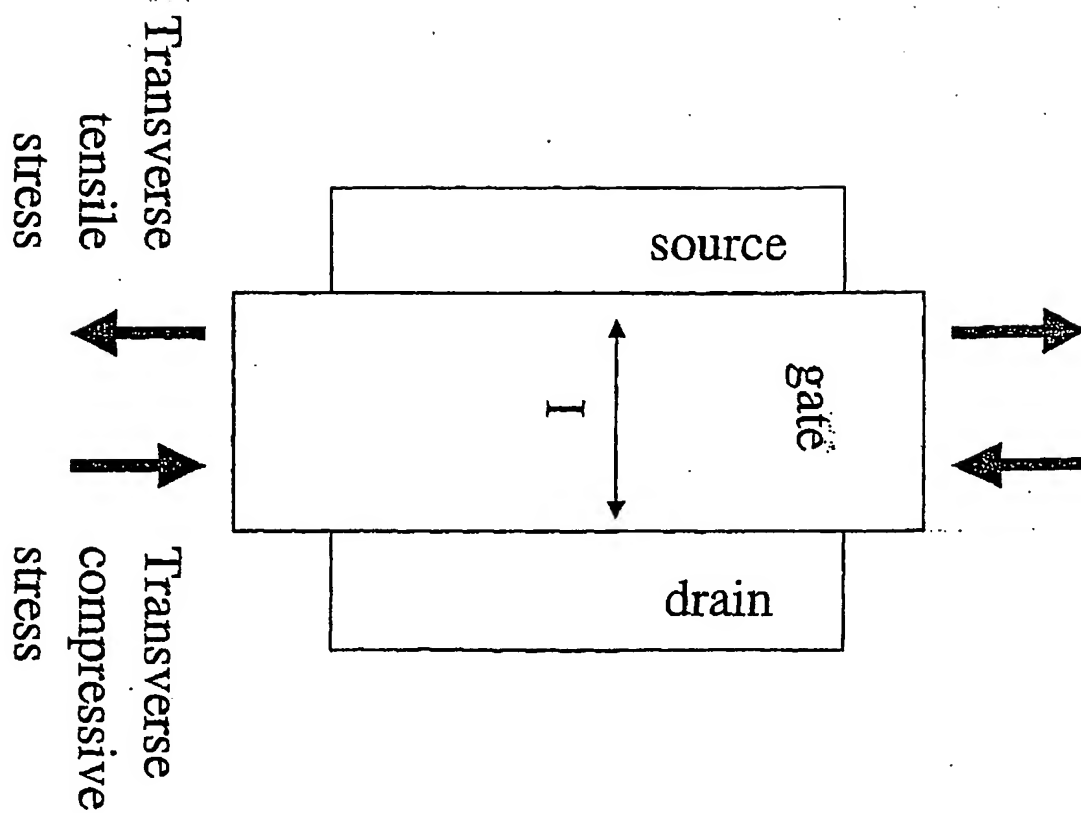


Figure 5

6/6

Figure 6



(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
6 June 2002 (06.06.2002)

PCT

(10) International Publication Number
WO 02/045156 A3

(51) International Patent Classification⁷: **H01L 21/8238**,
27/092

(21) International Application Number: **PCT/US01/44162**

(22) International Filing Date:
6 November 2001 (06.11.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/727,296 29 November 2000 (29.11.2000) US

(71) Applicant (for all designated States except US): **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **ARMSTRONG, Mark** [US/US]; 2861 NW Adagio Way, Hillsboro, OR 97124 (US). **SCHROM, Gerhard** [US/US]; 7008 NE

Ronler Way, #3225, Hillsboro, CA 97124 (US). **KUHN, Kelin, J.** [US/US]; 20280 SW Clarion Street, Aloha, OR 97006 (US). **PACKAN, Paul, A.** [US/US]; 15025 SW Gihtractar Court, Beaverton, OR 97007 (US). **TYAGI, Sunit, D.** [IN/US]; 17555 NW Waltnck Court, Portland, OR 97229 (US). **THOMPSON, Scott, E.** [US/US]; 18635 NW Rock Creek Way, Portland, OR 97229 (US).

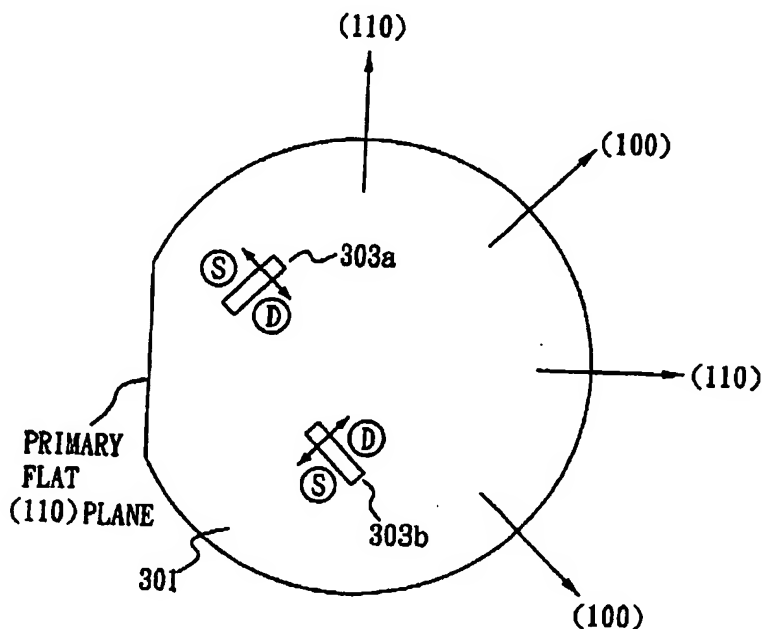
(74) Agents: **MALLIE, Michael, J.** et al.; Blakely, Sokoloff, Taylor & Zafman, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, CA 90025 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GH, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European

[Continued on next page]

(54) Title: CMOS FABRICATION PROCESS UTILIZING SPECIAL TRANSISTOR ORIENTATION



(57) Abstract: Complementary metal oxide semiconductor transistors are formed on a silicon substrate. The substrate has a {100} crystallographic orientation. The transistors are formed on the substrate so that current flows in the channels of the transistors are parallel to the <100> direction. Additionally, longitudinal tensile stress is applied to the channels.

WO 02/045156 A3



patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(88) Date of publication of the international search report:
23 January 2003

Published:

with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/44162

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/8238 H01L27/092

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 171 703 A (LIN YI-CHING ET AL) 15 December 1992 (1992-12-15) abstract; claims; figure 8 column 5, line 3 - line 8 column 9, line 48 - line 53 column 10, line 9 - line 11	1,2,6, 10,11
X	MATSUDA T ET AL: "ELECTRICAL CHARACTERISTICS OF Oølash;/+45ølash;/90ølash;-ORIEN TATION CMOSFET WITHSOURCE/DRAIN FABRICATED BY VARIOUS ION-IMPLANTATION METHODS" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE INC. NEW YORK, US, vol. 46, no. 4, April 1999 (1999-04), pages 703-711, XP000906406 ISSN: 0018-9383 abstract; figure 1	1,2,6, 10,11

-/-

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *B* document member of the same patent family

Date of the actual completion of the international search

26 August 2002

Date of mailing of the international search report

30/08/2002

Name and mailing address of the ISA

European Patent Office, P.B. 5816 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl
Fax: (+31-70) 340-8016

Authorized officer

Wirner, C

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 01/44162

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>SAYAMA H ET AL: "EFFECT OF CHANNEL DIRECTION FOR HIGH PERFORMANCE SCE IMMUNE PMOSFET WITH LESS THAN 0.15UM GATE LENGTH"</p> <p>INTERNATIONAL ELECTRON DEVICES MEETING 1999. IEDM. TECHNICAL DIGEST. WASHINGTON, DC, DEC. 5 - 8, 1999, NEW YORK, NY: IEEE, US,</p> <p>1 August 2000 (2000-08-01), pages 657-660, XP000933266</p> <p>ISBN: 0-7803-5411-7</p> <p>the whole document</p>	1,2,6, 10,11
Y		3-5,7-9, 12-15
Y	<p>WELSER J ET AL: "Strain dependence of the performance enhancement in strained-Si n-MOSFETs"</p> <p>ELECTRON DEVICES MEETING, 1994. TECHNICAL DIGEST., INTERNATIONAL SAN FRANCISCO, CA, USA 11-14 DEC. 1994, NEW YORK, NY, USA, IEEE,</p> <p>11 December 1994 (1994-12-11), pages 373-376, XP010131874</p> <p>ISBN: 0-7803-2111-1</p> <p>abstract; figure 1</p> <p>page 373, left-hand column, paragraph 2</p>	3,4,7,9, 12-14
Y	<p>SCOTT G ET AL: "Effect of stress and dopant redistribution on trench-isolated narrow devices"</p> <p>CHALLENGES IN PROCESS INTEGRATION AND DEVICE TECHNOLOGY, SANTA CLARA, CA, USA, 18-19 SEPT. 2000,</p> <p>vol. 4181, pages 183-190, XP008006927</p> <p>Proceedings of the SPIE - The International Society for Optical Engineering, 2000, SPIE-Int. Soc. Opt. Eng. USA</p> <p>ISSN: 0277-786X</p> <p>abstract; table 1</p> <p>page 186, paragraph 3 -page 187, paragraph 1</p>	5,8,15
A	<p>EP 0 703 628 A (MOTOROLA INC)</p> <p>27 March 1996 (1996-03-27)</p> <p>abstract; claims; figures</p>	1,3,4,7, 9,10, 12-14

-/-

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/44162

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SCOTT G ET AL: "NMOS drive current reduction caused by transistor layout and trench isolation induced stress" ELECTRON DEVICES MEETING, 1999. IEDM TECHNICAL DIGEST. INTERNATIONAL WASHINGTON, DC, USA 5-8 DEC. 1999, PISCATAWAY, NJ, USA, IEEE, US, 5 December 1999 (1999-12-05), pages 827-830, XP010372197 ISBN: 0-7803-5410-9 abstract	1,5,7,8, 10,12-15
A	US 6 046 494 A (CHAU ROBERT S ET AL) 4 April 2000 (2000-04-04) abstract; claims; figures	1,5,7,8, 10,12-15
A	GB 1 222 251 A (THOMSON CSF) 10 February 1971 (1971-02-10) abstract; claims; figures page 1, line 54 -page 2, line 25	1,3,4,7, 9,10, 12-14
A	GB 928 562 A (WESTERN ELECTRIC CO) 12 June 1963 (1963-06-12) abstract; claims; figures	1,3,4,7, 9,10, 12-14
A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 435 (E-825), 28 September 1989 (1989-09-28) -& JP 01 162362 A (FUJITSU LTD), 26 June 1989 (1989-06-26) abstract; figures	1,2,6, 10,12

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 01/44162

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5171703	A	15-12-1992	JP 5198543 A	06-08-1993
EP 0703628	A	27-03-1996	US 5561302 A	01-10-1996
			CN 1129358 A	21-08-1996
			EP 0703628 A2	27-03-1996
			JP 8111528 A	30-04-1996
			US 5683934 A	04-11-1997
US 6046494	A	04-04-2000	US 5633202 A	27-05-1997
GB 1222251	A	10-02-1971	FR 1522471 A	26-04-1968
			DE 1698122 A1	08-07-1971
			FR 2074759 A6	08-10-1971
			NL 6803482 A ,B,	16-09-1968
			US 3492861 A	03-02-1970
GB 928562	A	12-06-1963	BE 606275 A	
			DE 1232270 B	12-01-1967
			FR 1295244 A	01-06-1962
			NL 267220 A	
			US 3215568 A	02-11-1965
JP 01162362	A	26-06-1989	NONE	

Form PCT/ISA/210 (patent family annex) (July 1992)

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☒ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.